

#5/a  
V. Nguyen  
3/4/03  
002

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Azmoodeh

Application No.: 09/973,608

Filed: 10/9/2001

For: SYSTEMS AND METHODS FOR  
MINIMIZING HARMONIC  
INTERFERENCE

Examiner: An Luu

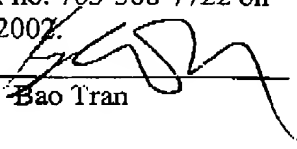
Art Unit: 2816

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RESPONSE

Assistant Commissioner for Patents  
Washington, D.C. 20231I certify that this response is being faxed to  
USPTO at fax no. 703-308-7722 on  
December 3, 2002.  
Bao Tran

Sir:

In response to the Office Action dated September 9, 2002, please amend the  
above-referenced application as follows.

## IN THE CLAIMS

Please replace the current set of claims with the following:

1. A method for minimizing nth-order harmonic associated with a square wave clock  
signal having a predetermined frequency and a duty cycle, comprising:
- changing the duty cycle of the clock to eliminate or suppress the nth-order  
harmonic of the clock; and
- generating a low-interference clock having the changed duty cycle while keeping  
the predetermined frequency.


5 TO: EXAMINER AN T LUU  
ART UNIT 2816

FROM: BAO TRAN

10 RE: Response for Serial No. 09/973,608

I certify that this response is being faxed to USPTO at fax no. 703-308-7722 on  
December 3, 2002.

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Bao Tran

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